Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2025

Third Semester

Electrical and Electronics Engineering

EE3302 – Digital Logic Circuits

Regulations - 2021

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Convert the number $(455)_{10}$ into binary format.	L3	1	2
2.	State De Morgan's theorem.	L1	1	2
3.	Which gates are called as the Universal gates? What are it advantages?	L2	2	2
4.	List the major applications of the multiplexers and decoders.	L2	2	2
5.	Differentiate between combinational and sequential circuits.	L2	3	2
6.	Draw the state diagram of the JK flip flop.	L2	3	2
7.	Define race condition in asynchronous sequential circuits.	L1	4	2
8.	Define PLA.	L1	4	2
9.	Write VHDL code for half adder in data flow model.	L2	5	2
10.	What are the types of simulation?	L2	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Show that ABC + ABC' + AB'C + A'BC = AB + AC + BC.	L3	1	8
		ii	Explain the operation of TTL NAND gate with a neat circuit diagram.	L3	1	8
			Or			
	b	i	Perform the following operation $(756)_8$ - $(437)_8$ + $(725)_{16}$. Express the answer in octal form.	L3	1	8
		ii	Explain the concept and implementation of ECL logic family.	L3	1	8
12.	a		Obtain the minimum SOP using K-map: $F=M_0+M_2+M_4+M_8+M_9+M_{10}+M_{11}+M_{12}+M_{13}$.	L3	2	16
			Or			
	b		Realize the Boolean function using 8:1 multiplexer: T=f (w,x,y,z) =m(0,1,2,4,5,7,8,9,12,13).	L3	2	16

13.	a	With neat diagram explain the working of bidirectional shift register.	L3	3	16
		Or			
	b	Design a synchronous mod 6 counter using T flip flops.	L3	3	16
14.	a	Design an asynchronous circuit that has two inputs x1 and x2 and one output z. The circuit is required to give an output whenever the input sequence (0,0), (0,1) and (1, 1) received but only in that order.	L3	4	16
		Or			
	b	Implement the following using PROM i) A(X,Y,Z) = $\sum_{max}(1,2,4,6)$ ii) B(X,Y,Z) = $\sum_{max}(0,1,6,7)$ iii) C(X,Y,Z) = $\sum_{max}(2,6)$	L3	4	16
15.	a i	Explain in detail about the RTL design procedure.	L3	5	8
	ii	Write a VHDL code to realize a 4x1 multiplexer.	L2	5	8
		Or			
	b i	Write short notes on packages.	L2	5	8
	ii	Write a VHDL code to realize a JK flip flop.	L2	5	8